**EAST WEST UNIVERSITY**

**Department of Computer Science and Engineering  
  
Semester:** Fall 2017  
**Course Number:** CSE345  
**Course Title:** Digital Logic Design

**Experiment Number:** 04  
**Experiment Title:** Binary Adder and Subtractor

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**Date of Performance:** October 30, 2017 **Date of Report Submission:** November 6, 2017

**Objective:**

1. To implement and test a full adder using random gates.

1. To test a 4-bit 2’s complement adder/subtractor using IC 7483 (4-bit binary parallel adder)

**Answer to the Post Lab Question:**

**01.**

Comparison between Experimental results and Pre-lab results:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Experimental result** | | **Prelab result** | |
|  |  |  |  |  |
| **0 0 0** | **0** | **0** | **0** | **0** |
| **0 0 1** | **0** | **1** | **0** | **1** |
| **0 1 0** | **0** | **1** | **0** | **1** |
| **0 1 1** | **1** | **0** | **1** | **0** |
| **1 0 0** | **0** | **1** | **0** | **1** |
| **1 0 1** | **1** | **0** | **1** | **0** |
| **1 1 0** | **1** | **0** | **1** | **0** |
| **1 1 1** | **1** | **1** | **1** | **1** |

These truth tables are same. So, results are verified.

**02.**

Structural Verilog code for full-adder:

**module expt2(input A, B, Cin,**

**output Sout, Cout);**

**wire w1, w2, w3, w4;**

**xor g1(w1, A, B),**

**g2(Sout, w1, Cin);**

**and g3(w3, A, B),**

**g4(w4, w1, Cin);**

**or g5(Cout, w3, w4);**

**endmodule**

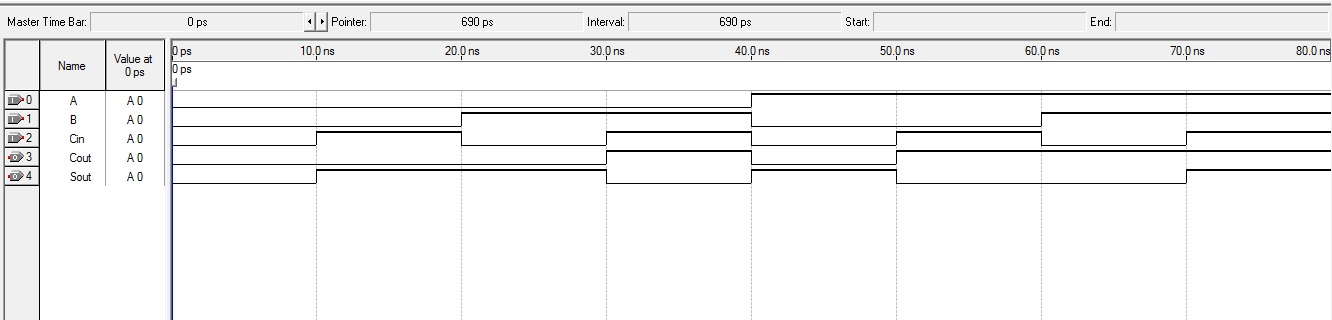
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Figure 1: Simulation Waveform

**03.**

Behavioral Verilog code for a 4- bit parallel adder:

**module expt3(output Cout,**

**output[3:0] S,**

**input[3:0] A, B,**

**input Cin);**

**assign {Cout, S} = A + B + Cin;**

**endmodule**

Example Inputs:

9+5,

9+6,

4+5,

9+2

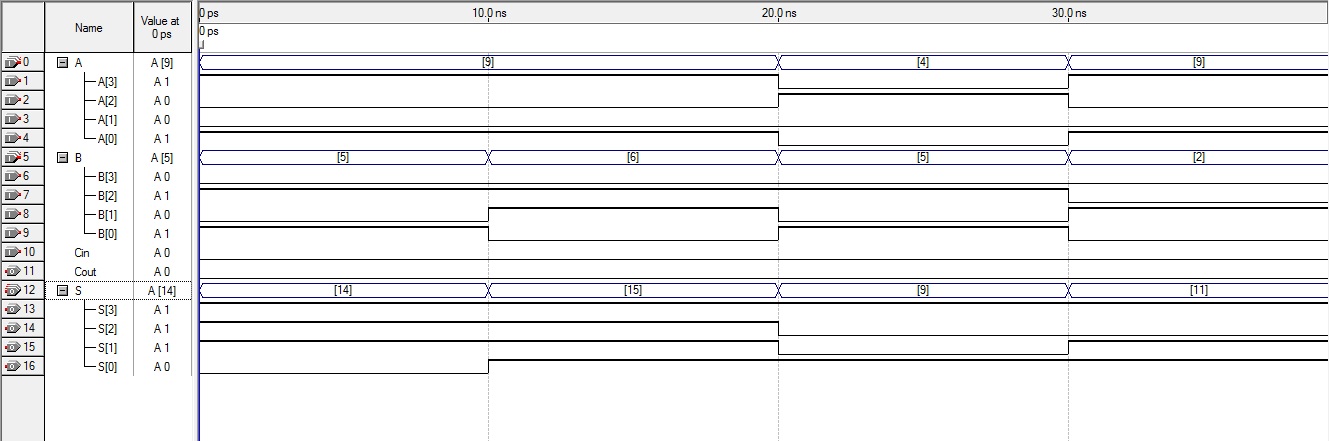
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Figure 2: Simulation waveform

**Conclusion:**

In this experiment, using IC 7483 we have learned how to implement a full adder and also test 4-bit 2’s complement. We write structural and behavioral Verilog code of these adders and used Quartus II software to perform simulation.